

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:
 - a semiconductor substrate having a first conductivity type;
 - a first well having a second conductivity type formed in a first region in a major surface of the semiconductor substrate;
 - a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well;
 - field oxide regions formed on a surface of the first well; and
 - a heavily doped region of buried layer having the second conductivity type formed in the first well at a distance away from the first contact region and the field oxide regions, wherein the distance is greater than 0, wherein the heavily doped region of buried layer prevents latch-up, wherein the heavily doped region of buried layer is not below a field oxide layer, and wherein said field oxide layer separates the first well and a second well.
2. (Previously Presented) The semiconductor device as claimed in claim 1, further comprising:

a second well having the first conductivity type formed in a second region in the major surface of the semiconductor substrate;

a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well; and

a heavily doped region of buried layer having the first conductivity type formed between the second contact region in the second well and a surface of the second well on an opposite portion of the second well from the second contact region within the semiconductor substrate.

3. (Previously Presented) The semiconductor device as claimed in claim 2, wherein the junction depth of the first and second wells is 1.5 to 2.0 μm .

4. (Previously Presented) The semiconductor device as claimed in claim 2, wherein the concentration of the heavily doped region of buried layer having the first conductivity type is higher than that of the second well and lower than that of the second contact region.

5-11. (Cancelled)

12. (Currently Amended) The semiconductor device as claimed in claim [[11]] 1, wherein the heavily doped region of the second conductivity type does not extend under the first MOS transistor in the first well.

13. (Previously Presented) The semiconductor device as claimed in claim 1, further comprising:

a second well having a first conductivity type formed in a second region of the semiconductor substrate, wherein a heavily doped region of buried layer having a first conductivity type is formed in the second well at a distance away from a second contact region and field oxide regions, wherein the distance is greater than 0.

14. (Previously Presented) The semiconductor device as claimed in claim 1, further comprising:

a second well having a first conductivity type formed in a second region of the semiconductor substrate; and

a heavily doped region of buried layer having a first conductivity type isolated within the second well and separated from boundaries that form the second well, wherein the distance between the heavily doped region having a first conductivity type and the boundaries of the second well is greater than 0.

15. (Currently Amended) A semiconductor device, comprising:
- a semiconductor substrate;
 - a first well having a second conductivity type formed in a first region of the semiconductor substrate;
 - a second well having a first conductivity type formed in a second region of the semiconductor substrate; [[and]]
 - field oxide regions formed on a surface of the second well, wherein a heavily doped region of buried layer having the first conductivity type is formed in the second well at a distance away from a second contact region and field oxide regions, wherein the distance is greater than 0; and
 - a heavily doped region of buried layer having a second conductivity type formed in the first well, wherein the heavily doped region is isolated within the first well and separated from boundaries that form the first well, wherein the distance between the heavily doped region and the boundaries that form the first well is greater than 0.

16. (Previously Presented) The semiconductor device as claimed in claim 15, further comprising:

field oxide regions formed on a surface of the first well, wherein the heavily doped region formed in the first well is formed at a distance away from the first contact region and the field oxide regions, wherein the distance is greater than 0.

17. (Previously Presented) The semiconductor device as claimed in claim 15, further comprising:

a heavily doped region of buried layer having a first conductivity type formed in the second well, wherein the heavily doped region is isolated within the second well and separated from boundaries that form the second well, wherein the distance between the heavily doped region and the boundaries that form the second well is greater than 0.

18. (Previously Presented) The semiconductor device as claimed in claim 17, wherein the concentration of the heavily doped region of buried layer having the first conductivity type is higher than that of the second well and lower than that of the second contact region.

19. (Previously Presented) The semiconductor device as claimed in claim 17, wherein the concentration of the heavily doped region of buried layer having the second conductivity type is higher than that of the first well and lower than that of the first contact region.

20. (Cancelled)

21. (Previously Presented) The semiconductor device as claimed in claim 15, wherein the heavily doped region of buried layer having a second conductivity type is formed not below a field oxide layer separating the first and second wells.

22. (Previously Presented) The semiconductor device as claimed in claim 15, further comprising:

a heavily doped region of buried layer having the first conductivity type formed in the second well, wherein the heavily doped region of buried layer having the first conductivity type is not formed below a field oxide layer separating the first and second wells.

23. (Currently Amended) The semiconductor device as claimed in claim ~~[[20]]~~ 15, wherein the heavily doped region of the second conductivity type does not extend under a first MOS transistor in the first well.

24. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate having a first conductivity type;

a first well having a second conductivity type formed in a first region of the semiconductor substrate;

a second well having the first conductivity type formed in a second region of the semiconductor substrate;

a field oxide layer formed on a portion of the semiconductor substrate where the first well and the second well contact one another;

a heavily doped region of buried layer having the second conductivity type formed in the first well; and

a heavily doped region of buried layer having the first conductivity type formed in the second well, wherein the heavily doped regions of buried layer of the first ~~and/or~~ conductivity type, the second conductivity type, or the first and second conductivity type is/are not below the field oxide layer.

25. (Cancelled)

26. (Previously Presented) The semiconductor device as claimed in claim 1, wherein the heavily doped region of buried layer is located within the first well isolated within the first well and separated from boundaries that form the first well, wherein the distance between the heavily doped region in the first well and the boundaries of the first well is greater than 0.

27. (Cancelled)

28. (Cancelled)

29. (Previously Presented) The semiconductor device as claimed in claim 15, wherein the heavily doped region of buried layer prevents latch-up.

30. (Previously Presented) The semiconductor device as claimed in claim 24, wherein each of the buried layers are isolated within each well and separated from boundaries that form each well, wherein the distance between each of the buried layers and the boundaries of each of the wells is greater than 0.

31. (Previously Presented) The semiconductor device as claimed in claim 24, wherein each of the heavily doped regions of buried layer prevent latch-up.

32. (Previously Presented) The semiconductor device as claimed in claim 24, further comprising:

field oxide regions formed on a surface of the first well and/or the second well, wherein the heavily doped region formed in the first well and/or the second well is formed at

a distance away from a first and/or a second contact region, respectively, and field regions, and wherein the distance is greater than 0.

33. (Previously Presented) The semiconductor device as claimed in claim 24, wherein at least one of the heavily doped regions of buried layer having a first conductivity type and/or second conductivity type is isolated within the second and/or the first well, respectively, and separated from boundaries that form the second well and/or the first well, respectively, wherein the distance between the heavily doped region having the first conductivity type and the boundaries of the second well is greater than 0 and/or the distance between the heavily doped region having the second conductivity type and the boundaries of the first well is greater than 0.

34. (Previously Presented) The semiconductor device as claimed in claim 24, wherein the heavily doped region having the second conductivity type is separated from a first contact region.

35. (Previously Presented) A semiconductor device, comprising:
a semiconductor substrate having a first conductivity type;

a first well having a second conductivity type formed in a first region of the semiconductor substrate; and

a heavily doped region of buried layer formed in the first well having a second conductivity type, wherein the heavily doped region is separated from a first contact region, and wherein the heavily doped region does not extend under a first MOS transistor in the first well.

36. (Previously Presented) The semiconductor device as claimed in claim 35, further comprising:

field oxide regions formed on a surface of the first well, wherein the heavily doped region formed in the first well is formed at a distance away from the first contact region and field oxide regions, wherein the distance is greater than 0.

37. (Previously Presented) The semiconductor device as claimed in claim 35, wherein the heavily doped region of buried layer is located within the first well, isolated within the first well and separated from boundaries that form the first well, wherein the distance between the heavily doped region in the first well and the boundaries of the first well is greater than 0.

38. (Previously Presented) The semiconductor device as claimed in claim 35, further comprising a second well in a second region of the semiconductor substrate, wherein the heavily

doped region of buried layer formed in the first well having a second conductivity type is formed not below a field oxide layer separating the first well and a second well.

39. (New) A semiconductor device comprising:
- a semiconductor substrate having a first conductivity type;
 - a first well having a second conductivity type formed in a first region in a major surface of the semiconductor substrate;
 - a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well;
 - field oxide regions formed on a surface of the first well; and
 - a heavily doped region of buried layer having the second conductivity type formed in the first well at a distance away from the first contact region and the field oxide regions, wherein the distance is greater than 0, wherein the heavily doped region of buried layer is located within the first well isolated within the first well and separated from boundaries that form the first well, wherein the distance between the heavily doped region in the first well and the boundaries of the first well is greater than 0.

40. (New) A semiconductor device, comprising:
- a semiconductor substrate;

a first well having a second conductivity type formed in a first region of the semiconductor substrate;

a second well having a first conductivity type formed in a second region of the semiconductor substrate; [[and]]

a heavily doped region of buried layer having a second conductivity type formed in the first well, wherein the heavily doped region is isolated within the first well and separated from boundaries that form the first well, wherein the distance between the heavily doped region and the boundaries that form the first well is greater than 0[[.]]; and

a heavily doped region of buried layer having a first conductivity type formed in the second well, wherein the heavily doped region is isolated within the second well and separated from boundaries that form the second well, wherein the distance between the heavily doped region and the boundaries that form the second well is greater than 0.